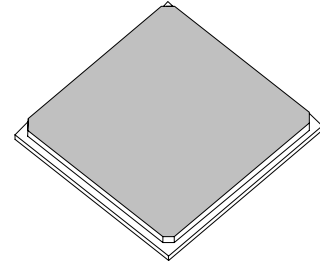


21 Channel E1/T1 Mapper

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OVERVIEW

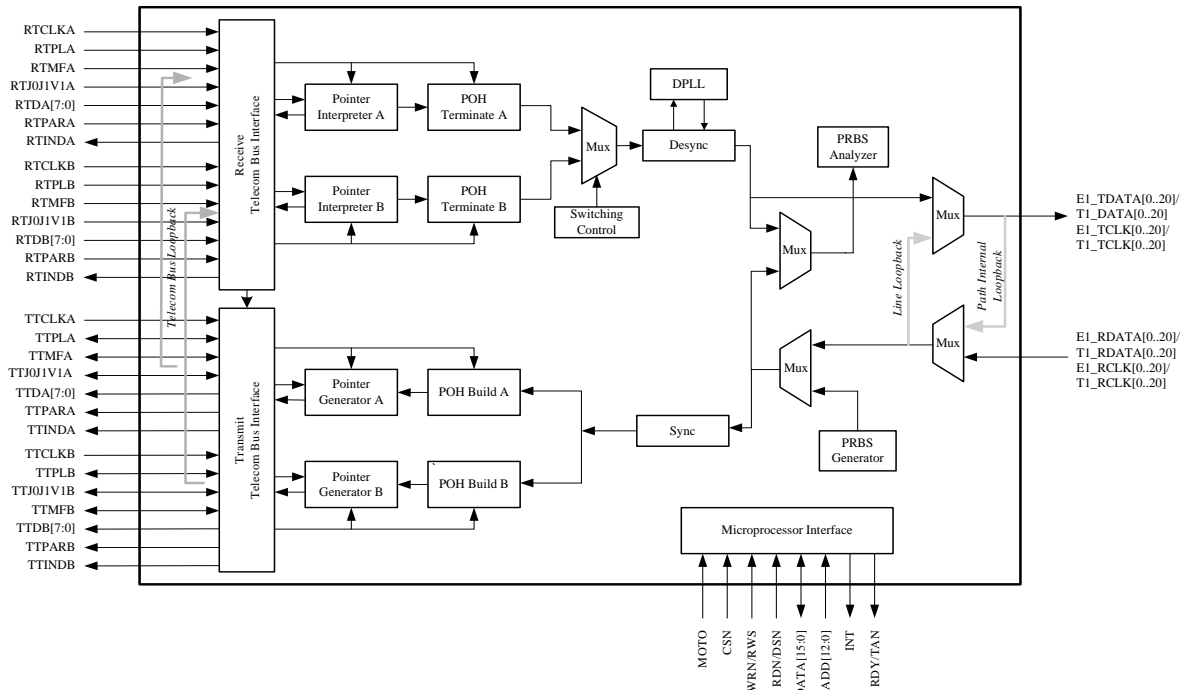
The CP1181 is one of the OPTRANS series chips designed by Chiphomer Technology Limited. It is designed for add/drop multiplexer, terminal multiplexer, dual and single unidirectional ring applications. 21 E1/T1 signals are mapped to and from asynchronous TU12. The CP1181 interfaces to a byte-wide 19.44 MHz Telecom Bus.



TEBGA256
-40 ~ 85°C

FEATURES

- Asynchronously mapping/de-mapping 21 E1 or T1 traffics into/from STM-1. T1 traffic mapping path is T1→VC11→ TU12.
- Configurable receive and transmit TU12 time-slots via microprocessor
- Detects loss of input clock on Telecom Bus
- Interprets TU12 pointer according to G.783 (2000/10) and G.707 (2000/10)
- Detects LOM, TU-LOP and TU-AIS alarms
- Detects Remote Defect Indication (RDI), Remote Error Indication (REI), RFI alarm and Path Label Mismatch (PLM) alarm
- Provides 12-bit performance counters for BIP-2 errors and 11-bit performance counters for tributary REI errors
- Detects degraded signals(DEG) and Excessive Error defects (EXC) based on received BIP-2 errors.
- Extracts the 16-byte J2 sequence into microprocessor accessible registers, and checks the J2 sequence to detect TIM alarm
- Detects the K4 (bit5-bit7) and V5 bit8 for Enhanced Defect Indicator (E-RDI)
- Captures filtered K4 byte into microprocessor accessible registers
- Extracts V5 and K4 bytes into microprocessor accessible registers
- Extracts N2 byte and O bits into microprocessor accessible registers



21 Channel E1/T1 Mapper

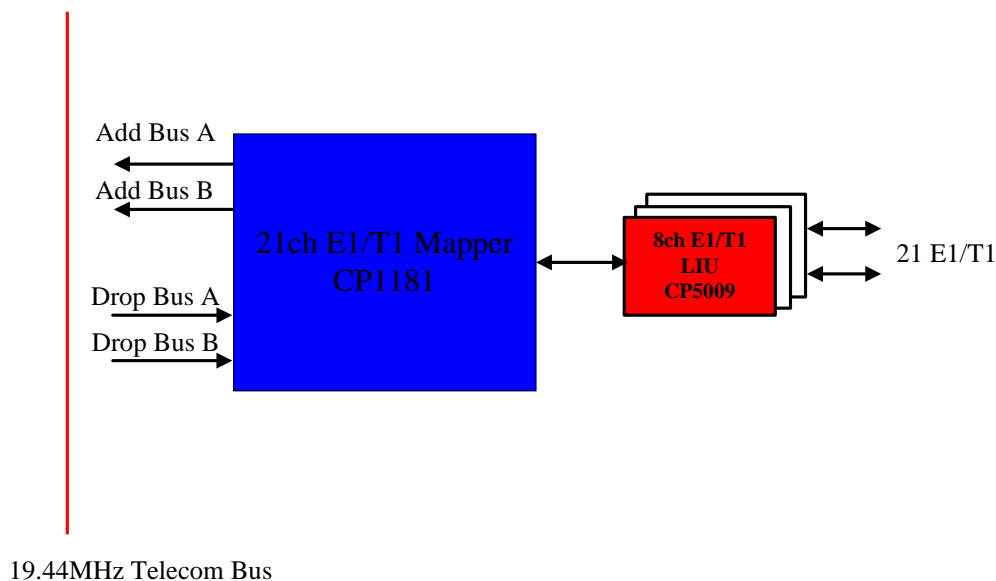
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- Supports 1+1 Path-protection
- Integrated bit-leaking circuit and DPLL
- The output jitter of E1/T1 data (either mapping jitter or combined jitter) is compliant with G.783 (2000/10)
- E1/T1 Port #0 to Port #7 can be configured to work in re-timing mode
- Supports the code-rate adjustment
- Optionally inserts VC-AIS and TU-AIS into upstream data
- Generates the TU12 pointer (V1, V2) per ITU G.783
- The TU12 pointer value is fixed on 105
- Calculates the BIP-2 and inserts into outgoing data stream, optionally inserts single or continued BIP-2 errors
- Inserts RDI/REI from either internal generation or microprocessor
- Inserts 16-byte programmable J2 sequence
- Inserts E-RDI from either internal generation or microprocessor
- Inserts programmable N2 byte and O bits
- Controlled High-Z output on transmit Telecom Bus
- Provides three bus timing modes for transmit Telecom Bus
- Build-in PRBS test function can be configured to any one of all 21 E1/T1 ports
- Provides 16-bit Intel/Motorola microprocessor interface
- 3.3V supply with 5V tolerant I/O
- IEEE 1149.1 JTAG boundary scan
- Maximum power less than 1.0 Watt
- Operating industrial temperature range: -40°C ~ 85°C
- PBGA256 package

APPLICATIONS

- SDH Add/Drop Multiplexers
- SDH Terminal Multiplexers
- Multi-service Transport Platform (MSTP)

TYPICAL APPLICATION



21 Channel E1/T1 MapperCP1181_PB_Rev1.0 March, 2005

RELATED PRODUCTS

- CH5008: 8ch E1 LIU
- CP5009: 8ch E1/T1/J1 LIU
- CP1122: STM-1 Single Chip Add/Drop Multiplexer System device
- CP1121: STM-1/4 Single Chip Add/Drop Multiplexer System device



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